UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	2666.72
First Named Inventor or Application Identifier	Runsheng HE
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification — *Total Pages* 21
3. [X] Drawing(s) *(35 USC 113)* — *Total Sheets* 9
4. [X] Oath or Declaration — *Total Pages* 2
   - a. [X] Newly executed (original or copy)
   - b. [ ] Unexecuted for information purposes
   - c. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
     - i. [ ] DELETION OF INVENTOR(S) — Signed Statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4c is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4c, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Two **(2)** Assignment Papers (cover sheet & document(s))
9 [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [X] Small Entity Statement(s) [ ] Statement filed in prior application Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other: ____________________

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information:*
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No. ________

18. CORRESPONDENCE ADDRESS

[X] Customer Number or Bar Code Label — 05514 (Insert Customer No. or Attach bar code label here) — or [ ] Correspondence address below

NAME					
Address					
City		State		Zip Code	
Country		Telephone		Fax	

JC715 U.S. PTO 08/24/00

jc864 U.S. PTO 09/644532 08/24/00

CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS (37 CFR 1.16(c))	74-20 =	54	X $ 18.00 =	$ 972.00
	INDEPENDENT CLAIMS (37 cfr 1.16(b))	4-3 =	1	X $ 78.00 =	$ 78.00
	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 CFR 1.16(d))			$ 260.00 =	$
				BASIC FEE (37 CFR 1.16(a))	$ 690.00
			Total of above Calculations =		$1740.00
	Reduction by 50% for filing by small entity (Note 37 CFR 1.9, 1.27, 1.28).				$870.00
				TOTAL =	$870.00

19. Small entity status

a. [X] A Small entity statement is enclosed.

b. [ ] A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.

c. [ ] Is no longer claimed.

20. [X] A check in the amount of $ 870.00 to cover the filing fee is enclosed.

21. [X] Two checks, each in the amount of $ 40.00, to cover the recordal fees are enclosed.

22. The Commissioner is hereby authorized to credit overpayments or charge the following fees to Deposit Account No. 06-1205:

a. [X] Fees required under 37 CFR 1.16.

b. [ ] Fees required under 37 CFR 1.17.

c. [ ] Fees required under 37 CFR 1.18.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED	
NAME	Steven W. Stewart - Reg. No. 45,133
SIGNATURE	St S
DATE	August 24, 2000

SWS/cob

STATEMENT CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) & 1.27(c)—SMALL BUSINESS CONCERN

DOCKET NUMBER: **MP0072**

Applicant, Patentee, or Identifier: **Runsheng He**
Application or Patent No.
Filed or Issued:
Title: **Feedforward Equalizer for DFE Based Detector**

I hereby state that I am
____ the owner of the small business concern identified below:
_X_ an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF SMALL BUSINESS CONCERN: Marvell Technology Group Ltd.
ADDRESS OF SMALL BUSINESS CONCERN: Richmond House, 3rd floor, 12 Parla Ville Road, Hamilton HM DX, Bermuda.

I hereby state that the above identified small business concern qualifies as a small business concern as defined in 13 CFR Part 121 for purposes of paying reduced fees to the United States Patent and Trademark Office. Questions related to size standards for a small business concern may be directed to: Small Business Administration, Size Standards Staff, 409 Third Street, SW, Washington, DC 20416.

I hereby state that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention described in:

_X_ the specification filed herewith with title as listed above.
____ the application identified above.
____ the patent identified above.

If the rights held by the above identified small business concern are not exclusive, each individual, concern, or organization having rights in the invention must file separate statements as to their status as small entities, and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern, or organization having any rights in the invention is listed below:
_X_ no such person, concern, or organization exists.
____ each such person, concern, or organization is listed below.

Separate statements are required from each named person, concern or organization having rights to the invention stating their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

NAME OF PERSON SIGNING Eric Janofsky
TITLE OF PERSON IF OTHER THAN OWNER General Patent Counsel
ADDRESS OF PERSON SIGNING 645 Almanor Avenue, Sunnyvale, CA 94086
SIGNATURE ______ DATE 8/24/00

MP0072

APPLICATION

FOR

UNITED STATES LETTERS PATENT

Be it known that I, Runsheng He, a citizen of the People's Republic of China, have invented new and useful improvements in:

FEEDFORWARD EQUALIZER FOR DFE BASED DETECTOR

of which the following is the specification.

FEEDFORWARD EQUALIZER FOR DFE BASED DETECTOR

Inventor: Runsheng He

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates generally to a feedforward equalizer used in conjunction with a decision feedback equalizer in a data communications channel. More particularly the present invention relates to a feedforward equalizer used in conjunction with a decision feedback equalizer for a gigabit Ethernet transceiver.

Description of the Related Art

A feedforward equalizer is an extremely useful component of a digital signal processor used to shape and otherwise to filter an input signal so as to obtain an output signal with desired characteristics. Feedforward equalizers may be used in such diverse fields as Ethernet transceivers, read circuits for disk drives, ghost cancellation in broadcast and cable TV transmission, channel equalization for communication in magnetic recording, echo cancellation, estimation/prediction for speech processing, adaptive noise cancellation, etc.

A feedforward equalizer is particularly suited for filtering inter-symbol interference (ISI). To varying degrees, ISI is always present in a data communications system. ISI is the result of the transmission characteristics of the communications channel, i.e., the "channel response," and, generally speaking, causes neighboring data symbols, in a transmission sequence, to spread out and interfere with one another. If the channel response is bad, or severe, ISI becomes a major impediment to having low error rate communications between two data endpoints. In fact, at higher data rates, i.e., frequencies, the affect of ISI is more severe since there is more high frequency attenuation in the transmission channel. Consequently, current efforts to push transmission speeds higher and higher in the local loop environment must effectively contend with ISI effects on a transmitted data signal to be successful.

Generally speaking the ISI can be divided into two components, namely precursor and post cursor ISI. Conventionally a feedforward equalizer (FFE) attempts to remove precursor ISI, and decision feedback equalization (DFE) attempts to remove

postcursor ISI. Fig. 1 is illustrative of a conventional feedforward equalizer used in conjunction with decision feedback equalizer in a data communications channel. As shown in Fig. 1, an analog, input signal from a communication channel is converted by to a digital signal by analog-to-digital converter 102. The digital signal is processed by FFE 104 and DFE 106 in a conventional manner. DFE 106 comprises decision circuit 108 and feedback filter 110. Examples of conventional arrangements are discussed in U.S. Patent Nos. 5,513,216 and 5,604,769, the contents of each of which are incorporated herein by reference.

However in conventional arrangements the length of the postcursor ISI is rather large, as shown in Fig. 2. To process a signal with a long tail, the feedback filter needs to have a proportionately large number of taps. This results in higher complexity and severe error progation.

Summary of the Invention

According to a first aspect of the present invention, a signal processing apparatus comprises an input circuit to receive an input signal. A feedforward equalizer comprises a high-pass filter and is responsive to the input circuit. A decision feedback equalizer comprises a decision circuit responsive to the feed forward equalizer and a feedback filter responsive to the decision circuit. The decision circuit is responsive to the feedback filter.

According to a second aspect of the present invention, the high-pass filter has a low cutoff frequency.

According to a third aspect of the present invention, the high-pass filter has a flat response.

According to a fourth aspect of the present invention, the high-pass filter has high attenuation at low frequency.

According to a fifth aspect of the present invention, the high-pass filter has high attenuation at low frequencies.

According to a sixth aspect of the present invention, the high attenuation is at least 20 db.

According to a seventh aspect of the present invention, the high-pass filter comprises a first finite impulse response filter (FIR).

According to an eighth aspect of the present invention, the first FIR filter comprises M taps to filter precursor ISI, one main tap and N taps to filter postcursor ISI.

According to a ninth aspect of the present invention, each tap of the first FIR filter has a corresponding coefficient W as follows:

W_0 = unity

$$0 < \sum_{1}^{M} W_{-i} + W_o + \sum_{1}^{n} W_i << 1, \text{ and}$$

$-1 << W_1, \ldots W_n << 0.$

According to a tenth aspect of the present invention, the input circuit comprises an analog to digital converter.

According to an eleventh aspect of the present invention, the decision circuit comprises a threshold circuit.

According to a twelfth aspect of the present invention, the decision circuit comprises a Viterbi detector.

According to a thirteenth aspect of the present invention, a first adaptive control circuit is provided to adapt the M taps for filtering precursor ISI and N taps for filtering.

According to a fourteenth aspect of the present invention, each of the N taps comprises a limiter to limit the range of adaptation of the N taps.

According to a fifteenth aspect of the present invention, the first adaptive control circuit is operable only during signal acquisition.

According to a sixteenth aspect of the present invention, the feedback filter comprises a second finite impulse response filter (FIR).

According to a seventeenth aspect of the present invention, a second adaptive control circuit to adapt taps of the second FIR.

According to an eighteenth aspect of the present invention, a signal processing apparatus comprises an input means for receiving an input signal. A feedforward equalizer means is provided for feedforward equalizing by high-pass filtering the input signal received by the input means. A decision feedback equalizer means comprises a decision means for recovering data from an output of the feedforward equalizer means

and a feedback filter means for filtering an output of the decision means. The decision means is responsive to the feedback filter means.

According to a nineteenth aspect of the present invention, the feedforward equalizer means has a low cutoff frequency.

According to a twentieth aspect of the present invention, the feedforward equalizer means has a flat response.

According to a twenty-first aspect of the present invention, the feedforward equalizer means has high attenuation at low frequency.

According to a twenty-second aspect of the present invention, the feedforward equalizer means has high attenuation at low frequencies.

According to a twenty-third aspect of the present invention, the feedforward equalizer means shortens a length of postcursor inter-symbol interference.

According to a twenty-fourth aspect of the present invention, the feedforward equalizer means attenuates any DC noise.

According to a twenty-fifth aspect of the present invention, the feedforward equalizer means attenuates baseline wander.

According to a twenty-sixth aspect of the present invention, the high attenuation is at least 20 dB.

According to a twenty-seventh aspect of the present invention, the feedforward equalizer means comprises a first finite impulse response filter (FIR) means for filtering the input signal.

According to a twenty-eighth aspect of the present invention, the first FIR filter means comprises M taps for filtering precursor ISI, one main tap and N taps for filtering postcursor ISI.

According to a twenty-ninth aspect of the present invention, each tap of the first FIR filter means has a corresponding coefficient W as follows:

W_0 = unity

$$0 < \sum_{1}^{M} W_{-i} + W_o + \sum_{1}^{n} W_i << 1, \text{ and}$$

$-1 << W_1, \ldots W_n << 0.$

According to a thirtieth aspect of the present invention, the input means comprises an analog to digital converter means for converting an analog input signal to a digital signal.

According to a thirty-first aspect of the present invention, the decision means comprises a threshold circuit.

According to a thirty-second aspect of the present invention, the decision means comprises a Viterbi detector.

According to a thirty-third aspect of the present invention, a first adaptive control means is provided for adapting the M taps for filtering precursor ISI and N taps for filtering.

According to a thirty-fourth aspect of the present invention, each of the N taps comprises a limiting means for limiting the range of adaptation of the N taps.

According to a thirty-fifth aspect of the present invention, the first adaptive control means is operable only during signal acquisition.

According to a thirty-sixth aspect of the present invention, the feedback filter means comprises a second finite impulse response filter (FIR) means for filtering the output of the decision means.

According to a thirty-seventh aspect of the present invention, a second adaptive control means is provided for adapting taps of the second FIR means.

Other objects and attainments together with a fuller understanding of the invention will become apparent and appreciated by referring to the following description and claims taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

In the drawings wherein like reference symbols refer to like parts.

Fig. 1 is a block diagram of a feedforward equalizer used in conjunction with a decision feedback equalizer;

Fig. 2 illustratively shows the length of the postcursor ISI when an input signal is processed by a conventional arrangement;

Fig. 3 is a block diagram of a feedforward equalizer implemented as a high-pass filter used in conjunction with a decision feedback equalizer in accordance with a first embodiment of the present invention;

Fig. 4 illustratively shows the length of the postcursor ISI of when an input signal is processed by the present invention;

Fig. 5 illustrates the frequency response of the high-pass filter in accordance with Fig. 3;

Fig. 6 is a schematic drawing of the high-pass filter of Fig. 3 implemented as an finite impulse response (FIR) filter;

Fig. 7 is a block diagram of a feedforward equalizer implemented as an adaptive high-pass filter used in conjunction with a decision feedback equalizer in accordance with a second embodiment of the present invention;

Fig. 8 is a schematic drawing of the high-pass filter of Fig. 7 implemented as an adaptive finite impulse response (FIR) filter; and

Fig. 9 is a block diagram of an Ethernet transceiver incorporating the feedforward equalizer used in conjunction with a decision feedback equalizer in accordance with the present invention.

Description of the Preferred Embodiments

The present invention will now be described with reference with to a feedforward equalizer used in an Ethernet transceiver device. Preferably, the feedforward equalizer is embodied in an Integrated Circuit disposed between a digital interface and an RJ45 analog jack. The Integrated Circuit may be installed inside a PC on the network interface card or the motherboard, or may be installed inside a network switch or router. However, other embodiments include applications in read circuits for disk drives, ghost cancellation in broadcast and cable TV transmission, channel equalization for communication in magnetic recording, echo cancellation, estimation/prediction for speech processing, adaptive noise cancellation, etc. All such embodiments are included within the scope of the appended claims.

Moreover, while the invention will be described with respect to the functional elements of the FFE, the person of ordinary skill in the art will be able to embody such functions in discrete digital or analog circuitry, or as software executed by a general purpose process (CPU) or digital signal processor.

A functional block diagram of an Ethernet transceiver incorporating the FFE according to the present invention is depicted in Fig. 9. Although only one channel is

depicted therein, four parallel channels are typically used in Gigabit Ethernet applications. Only one channel is depicted and described herein for clarity.

A 125 MHz, 250Mbps digital input signal from a PC is PCS-encoded in a PCS encoder 2 and is then supplied to a D/A converter 4 for transmission to the Ethernet cable 6. The PCS-encoded signal is also supplied to a NEXT (Near End Transmitter) noise canceller 8 and to adaptive echo canceller 10.

Signals from the Ethernet cable 6 are received at adder 14 and added with correction signals supplied from baseline wander correction block 12 (which corrects for DC offset). The added signals are then converted to digital signals in the A/D converter 16, as controlled by timing and phase-lock-loop block 18. The digital signals from A/D converter 16 are supplied to delay adjustment block 20, which synchronizes the signals in accordance with the four parallel Ethernet channels. The delay-adjusted digital signals are then added with the echo-canceled signals and the NEXT-canceled signals in adder 22.

The added signals are supplied to a Feed Forward Equalizer filter 24 which filters the signal prior to DFE or more specifially ,Viterbi trellis decoding in decoder 26. After Viterbi decoding, the output signal is supplied to PCS decoder 28, after which the PCS-decoded signal is supplied to the PC.

The decoder 26 also supplies output signals to a plurality of adaptation blocks schematically depicted at 30 in Fig. 9. As is known, such adaptation blocks carry out corrections for such conditions as temperature offset, connector mismatch, etc. The adaptation block 30 provides output to the baseline wander correction circuit 12, the timing and phase-lock-loop circuit 18, the echo canceller 10, and the NEXT canceller 8. Each functional block depicted in Fig. 9 includes a slave state controller (not shown) for controlling the operation and timing of the corresponding block.

Reference is now made to Fig. 3 which shows a block diagram of a feedforward equalizer implemented as a high-pass filter used in conjunction with a decision feedback equalizer in accordance with a first embodiment of the present invention. As shown therein, an analog input signal is converted to a digital signal by analog-to-digital converter (ADC) 312. The FFE 304 processes the digitized input signal to effectively cancel the precursor ISI and shorten the length of the postcursor ISI. Fig. 4 illustratively shows the shorten length of the postcursor ISI of when an input signal is processed by FFE 304 of the present invention. FFE 304 is preferably implemented as a high-pass filter to shorten the tail. The output of FFE 304 is then processed by DFE

305 to effectively cancel the postcursor ISI in a known manner. DFE 305 comprises decision circuit 308 and feedback filter 310. Decision circuit 308 may be implemented by, for example, a threshold circuit, a Viterbi detector or the like. Feedback filter 310 is preferably implemented as a FIR filter.

Fig. 5 illustrates the response characteristics of high-pass filter of FFE 304. The filter has a low cutoff frequency. As can be seen in Fig. 5, at higher frequencies the filter has a relatively flat response and has high attenuation at low frequencies (preferably 20 db). This characteristic is advantageous in attenuating any DC noise and any DC components caused by baseline wander. Significantly, the flat response reduces noise enhancement.

Referring now to Fig. 6, high-pass filter 304 is preferably implemented as a finite impulse response (FIR) filter 600. FIR filter 600 comprises M taps for filtering precursor ISI, one main tap and N taps for filtering postcursor ISI. In the preferred embodiment M=1 and N=3. Each tap comprises a delay 602 (except for the first tap), a multiplier 604 and a summer 606 (except for the first tap). Delay circuit 602 delays an output from a previous tap, and multiplier 604 multiples the output from delay circuit 602 by a coefficient W. The output of multiplier 604 is added to an output from of previous tap by summer 606.

The selection of the coefficients W is critical in providing the response defined in Fig. 5. To achieve this response, the selection of the coefficients W is critical. The appropriate selection of coefficients $W_1 \ldots W_n$ determines the sharpness of the response, and the appropriate selection of coefficients W_{-m}-W_{-1} effectively cancels the precursor tail. In the present embodiment the coefficients are selected from the following constraints:

W_0 = unity

$$0 < \sum_{1}^{M} W_{-i} + W_o + \sum_{1}^{n} W_i << 1$$

$-1 << W_1, \ldots W_n << 0$,

in the preferred embodiment

$W_0=1$

$W_{-1}=-0.1$

$W_{-1}+W_0+W_1+W_2+W_3=0.1$

$|W_1| > |W_2| > |W_3|$

$-1 << W_1, W_2, W_3 << 0$, preferably $W_1=-.35$, $W_2=-.25$, and $W_3=-.20$.

As will be appreciated by one of ordinary skill in the art, the preferred values discussed above may be proportionately varied to still achieve very similar and acceptable responses.

Fig. 7 is an alternate embodiment of the present invention, in which the coefficients of the FIR of the FFE is adaptive and the FIR of the feedback filter is also adaptive. In general, an error generator circuit 724 is provided to determine any errors during signal acquisition, and an error signal is provided to an adaptive control circuit 720 to move the coefficients of the FFE. These coefficients of the FFE are only moved during signal acquisition. After acquisition, the coefficients of the FFE are then held at the values determined during acquisition. Also, an error generator 726 determines if there are any errors from feedback filter 110 and provides an error signal to adaptive control circuit 728. Adaptive control circuit 728 moves coefficients for feedback filter 110.

Fig. 8 shows a more detailed schematic of an adaptive FIR filter for FFE. As shown therein, the main tap W_0 is kept at its initial value and is not adapted. Coefficients $W_{-m} \ldots W_{-1}$ can be determined by LMS engines $840_m \ldots 840_{-1}$ in accordance with a least mean square (LMS) algorithm based on gradient optimization. The change in tap weight coefficients ΔWn is calculated to be $\Delta Wn = \Delta * Xn * En$; where Δ is the adaptation rate and E is the error output by the error generator 724. Coefficients $W_1 \ldots W_n$ are similarly determined by LMS engines $840_1 \ldots 840_n$. In addition limiters $830_1 \ldots 830_n$ are provided to enforce the constraints discussed above.

While the invention has been described in conjunction with several specific embodiments, it is evident to those skilled in the art that many further alternatives, modifications and variations will be apparent in light of the foregoing description. Thus, the invention described herein is intended to embrace all such alternatives, modifications, applications and variations as may fall within the spirit and scope of the appended claims.

WHAT IS CLAIMED IS:

1. A signal processing apparatus comprising:

an input circuit to receive an input signal;

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit; and

a decision feedback equalizer comprising:

a decision circuit responsive to said feed forward equalizer; and

a feedback filter responsive to said decision circuit, wherein said decision circuit is responsive to said feedback filter.

2. A signal processing circuit according to Claim 1, wherein said high-pass filter has a low cutoff frequency.

3. A signal processing circuit according to Claim 2, wherein said high-pass filter has a flat response.

4. A signal processing circuit according to Claim 1, wherein said high-pass filter has high attenuation at low frequency.

5. A signal processing circuit according to Claim 1, wherein said high-pass filter has high attenuation at low frequencies.

6. A signal processing circuit according to Claim 5, wherein the high attenuation is at least 20 db.

7. A signal processing circuit according to Claim 1, wherein said high-pass filter comprises a first finite impulse response filter (FIR).

8. A signal processing circuit according to Claim 7, wherein said first FIR filter comprises M taps to filter precursor ISI, one main tap and N taps to filter postcursor ISI.

9. A signal processing circuit according to Claim 8, wherein each tap of said first FIR filter has a corresponding coefficient W as follows:

W_0 = unity

$$0<\sum_{1}^{M} W_{-i}+W_0+\sum_{1}^{n} W_i<<1, \text{ and}$$

$-1<<W_1, \ldots W_n<<0.$

10. A signal processing circuit according to Claim 1, wherein said input circuit comprises an analog to digital converter.

11. A signal processing circuit according to Claim 1, wherein said decision circuit comprises a threshold circuit.

12. A signal processing circuit according to Claim 1, wherein said decision circuit comprises a Viterbi detector.

13. A signal processing circuit according to Claim 8, further comprising a first adaptive control circuit to adapt the M taps for filtering precursor ISI and N taps for filtering.

14. A signal processing circuit according to Claim 13, wherein each of the N taps comprises a limiter to limit the range of adaptation of the N taps.

15. A signal processing circuit according to Claim 13, wherein said first adaptive control circuit is operable only during signal acquisition.

16. A signal processing circuit according to Claim 1, wherein said feedback filter comprises a second finite impulse response filter (FIR).

17. A signal processing circuit according to Claim 15, further comprising a second adaptive control circuit to adapt taps of said second FIR.

18. A signal processing apparatus comprising:

input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means; and

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means, wherein said decision means is responsive to said feedback filter means.

19. A signal processing circuit according to Claim 18, wherein said feedforward equalizer means has a low cutoff frequency.

20. A signal processing circuit according to Claim 19, wherein said feedforward equalizer means has a flat response.

21. A signal processing circuit according to Claim 18, wherein said feedforward equalizer means has high attenuation at low frequency.

22. A signal processing circuit according to Claim 18, wherein said feedforward equalizer means has high attenuation at low frequencies.

23. A signal processing circuit according to Claim 18, wherein said feedforward equalizer means shortens a length of postcursor inter-symbol interference.

24. A signal processing circuit according to Claim 18, wherein said feedforward equalizer means attenuates any DC noise.

25. A signal processing circuit according to Claim 18, wherein said feedforward equalizer means attenuates baseline wander.

26. A signal processing circuit according to Claim 22, wherein the high attenuation is at least 20 db.

27. A signal processing circuit according to Claim 18, wherein said feedforward equalizer means comprises a first finite impulse response filter (FIR) means for filtering the input signal.

28. A signal processing circuit according to Claim 27, wherein said first FIR filter means comprises M taps for filtering precursor ISI, one main tap and N taps for filtering postcursor ISI.

29. A signal processing circuit according to Claim 28, wherein each tap of said first FIR filter means has a corresponding coefficient W as follows:

W_0 = unity

$0 < \sum_{1}^{M} W_{-i} + W_0 + \sum_{1}^{n} W_i << 1$, and

$-1 << W_1, \ldots W_n << 0$.

30. A signal processing circuit according to Claim 18, wherein said input means comprises an analog to digital converter means for converting an analog input signal to a digital signal.

31. A signal processing circuit according to Claim 18, wherein said decision means comprises a threshold circuit.

32. A signal processing circuit according to Claim 18, wherein said decision means comprises a Viterbi detector.

33. A signal processing circuit according to Claim 28, further comprising a first adaptive control means for adapting the M taps for filtering precursor ISI and N taps for filtering.

34. A signal processing circuit according to Claim 33, wherein each of the N taps comprises a limiting means for limiting the range of adaptation of the N taps.

35. A signal processing circuit according to Claim 33, wherein said first adaptive control means is operable only during signal acquisition.

36. A signal processing circuit according to Claim 18, wherein said feedback filter means comprises a second finite impulse response filter (FIR) means for filtering the output of said decision means.

37. A signal processing circuit according to Claim 36, further comprising a second adaptive control means for adapting taps of said second FIR means.

38. An Ethernet transceiver, comprising:

an input for inputting an input signal into an Ethernet cable;

an output for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit; and

a decision feedback equalizer comprising:

a decision circuit responsive to said feed forward equalizer; and

a feedback filter responsive to said decision circuit, wherein said decision circuit is responsive to said feedback filter.

39. An Ethernet transceiver according to Claim 38, wherein said high-pass filter has a low cutoff frequency.

40. An Ethernet transceiver according to Claim 39, wherein said high-pass filter has a flat response.

41. An Ethernet transceiver according to Claim 38, wherein said high-pass filter has high attenuation at low frequency.

42. An Ethernet transceiver according to Claim 38, wherein said high-pass filter has high attenuation at low frequencies.

43. An Ethernet transceiver according to Claim 42, wherein the high attenuation is at least 20 db.

44. An Ethernet transceiver according to Claim 38, wherein said high-pass filter comprises a first finite impulse response filter (FIR).

45. An Ethernet transceiver according to Claim 44, wherein said first FIR filter comprises M taps to filter precursor ISI, one main tap and N taps to filter postcursor ISI.

46. An Ethernet transceiver according to Claim 45, wherein each tap of said first FIR filter has a corresponding coefficient W as follows:

W0 = unity

$$0<\sum_{1}^{M} W_{-i}+W_o+\sum_{1}^{n} W_i<<1$$, and

$-1 << W1, \ldots Wn << 0$.

47. An Ethernet transceiver according to Claim 38, wherein said input circuit comprises an analog to digital converter.

48. An Ethernet transceiver according to Claim 38, wherein said decision circuit comprises a threshold circuit.

49. An Ethernet transceiver according to Claim 38, wherein said decision circuit comprises a Viterbi detector.

50. An Ethernet transceiver according to Claim 45, further comprising a first adaptive control circuit to adapt the M taps for filtering precursor ISI and N taps for filtering.

51. An Ethernet transceiver according to Claim 50, wherein each of the N taps comprises a limiter to limit the range of adaptation of the N taps.

52. An Ethernet transceiver according to Claim 50, wherein said first adaptive control circuit is operable only during signal acquisition.

53. An Ethernet transceiver according to Claim 38, wherein said feedback filter comprises a second finite impulse response filter (FIR).

54. An Ethernet transceiver according to Claim 53, further comprising a second adaptive control circuit to adapt taps of said second FIR.

55. A signal processing apparatus comprising:

input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means; and

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means, wherein said decision means is responsive to said feedback filter means.

56. An Ethernet transceiver according to Claim 55, wherein said feedforward equalizer means has a low cutoff frequency.

57. An Ethernet transceiver according to Claim 56, wherein said feedforward equalizer means has a flat response.

58. An Ethernet transceiver according to Claim 55, wherein said feedforward equalizer means has high attenuation at low frequency.

59. An Ethernet transceiver according to Claim 55, wherein said feedforward equalizer means has high attenuation at low frequencies.

60. An Ethernet transceiver according to Claim 55, wherein said feedforward equalizer means shortens a length of postcursor inter-symbol interference.

61. An Ethernet transceiver according to Claim 55, wherein said feedforward equalizer means attenuates any DC noise.

62. An Ethernet transceiver according to Claim 55, wherein said feedforward equalizer means attenuates baseline wander.

63. An Ethernet transceiver according to Claim 59, wherein the high attenuation is at least 20 db.

64. An Ethernet transceiver according to Claim 55, wherein said feedforward equalizer means comprises a first finite impulse response filter (FIR) means for filtering the input signal.

65. An Ethernet transceiver according to Claim 64, wherein said first FIR filter means comprises M taps for filtering precursor ISI, one main tap and N taps for filtering postcursor ISI.

66. An Ethernet transceiver according to Claim 65, wherein each tap of said first FIR filter means has a corresponding coefficient W as follows:

W_0 = unity

$0 < \sum_{1}^{M} W_{-i} + W_0 + \sum_{1}^{n} W_i << 1$, and

$-1 << W_1, \ldots W_n << 0$.

67. An Ethernet transceiver according to Claim 55, wherein said input means comprises an analog to digital converter means for converting an analog input signal to a digital signal.

68. An Ethernet transceiver according to Claim 55, wherein said decision means comprises a threshold circuit.

69. An Ethernet transceiver according to Claim 55, wherein said decision means comprises a Viterbi detector.

70. An Ethernet transceiver according to Claim 65, further comprising a first adaptive control means for adapting the M taps for filtering precursor ISI and N taps for filtering.

71. An Ethernet transceiver according to Claim 33, wherein each of the N taps comprises a limiting means for limiting the range of adaptation of the N taps.

72. An Ethernet transceiver according to Claim 70, wherein said first adaptive control means is operable only during signal acquisition.

73. An Ethernet transceiver according to Claim 55, wherein said feedback filter means comprises a second finite impulse response filter (FIR) means for filtering the output of said decision means.

74. An Ethernet transceiver according to Claim 73, further comprising a second adaptive control means for adapting taps of said second FIR means.

ABSTRACT

A feedforward equalizer for DFE based detector is provided comprising a digital to analog converter to convert an analog signal to a digital signal. A feedforward equalizer comprises a high-pass filter and is responsive to the input circuit. The high-pass filter has a low cutoff frequency, has a relatively flat response and has high attenuation at low frequencies. A decision feedback equalizer comprises a decision circuit responsive to the feedforward equalizer, and a feedback filter is responsive to the decision circuit. The decision circuit is also responsive to the feedback filter.

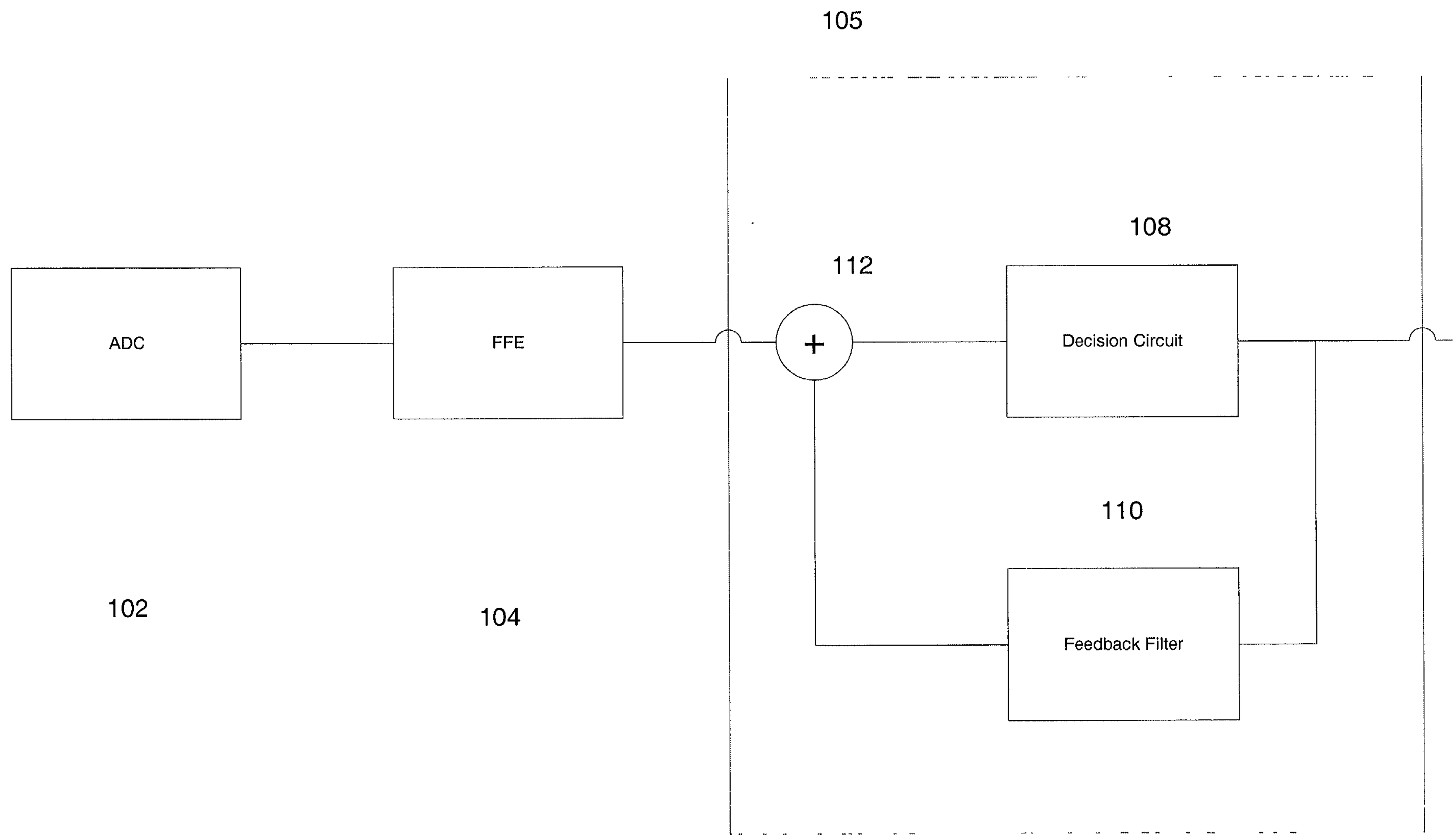
105
112
108
ADC
FFE
+
Decision Circuit
110
Feedback Filter
102
104

Fig. 1

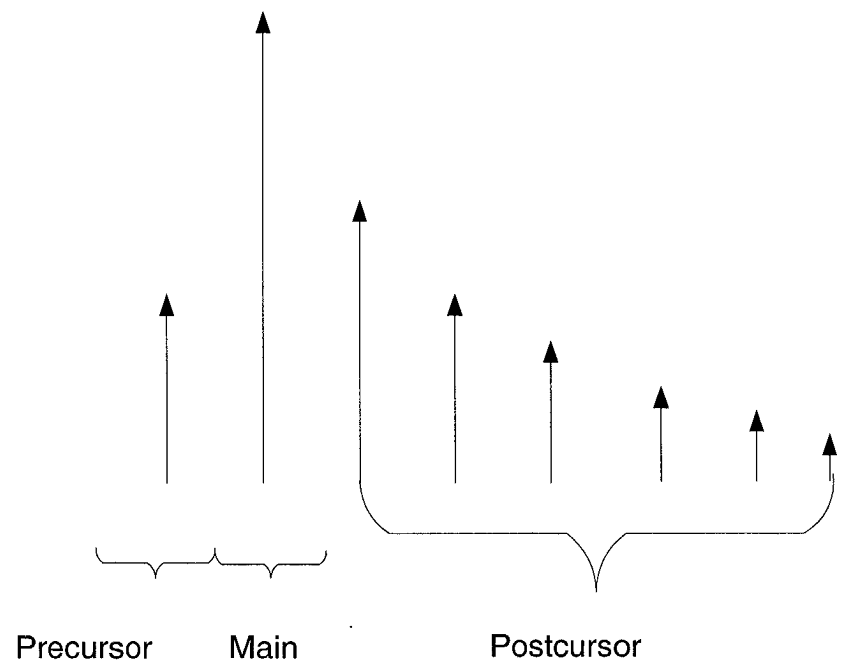

Fig. 2

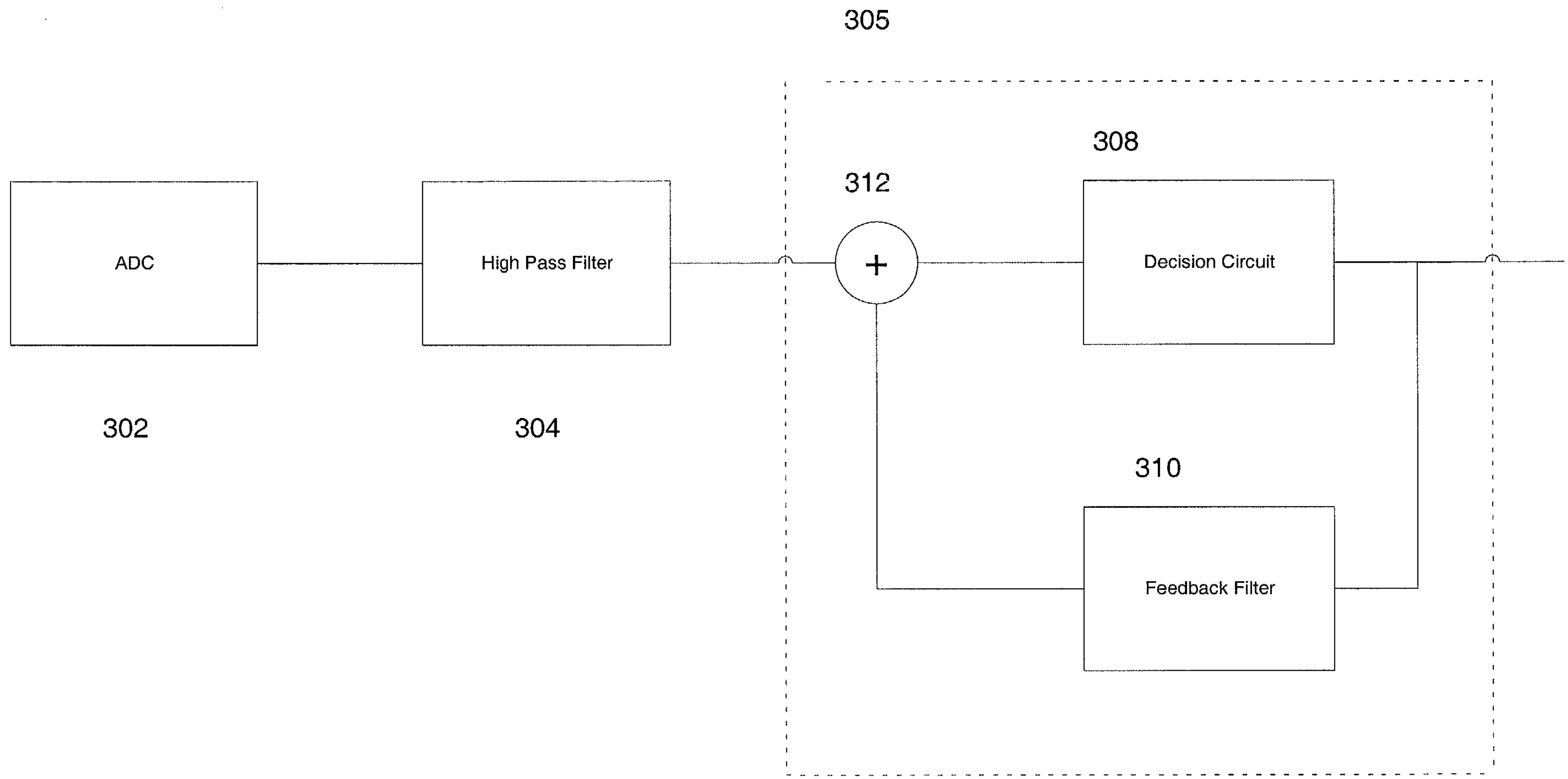
305
308
312
ADC
High Pass Filter
+
Decision Circuit
302
304
310
Feedback Filter

Fig. 3

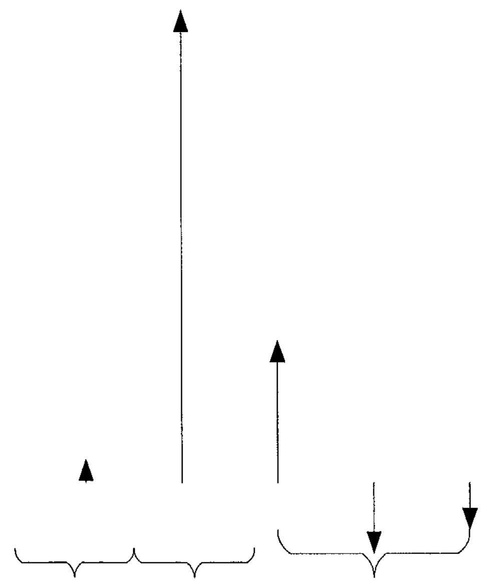

Fig. 4

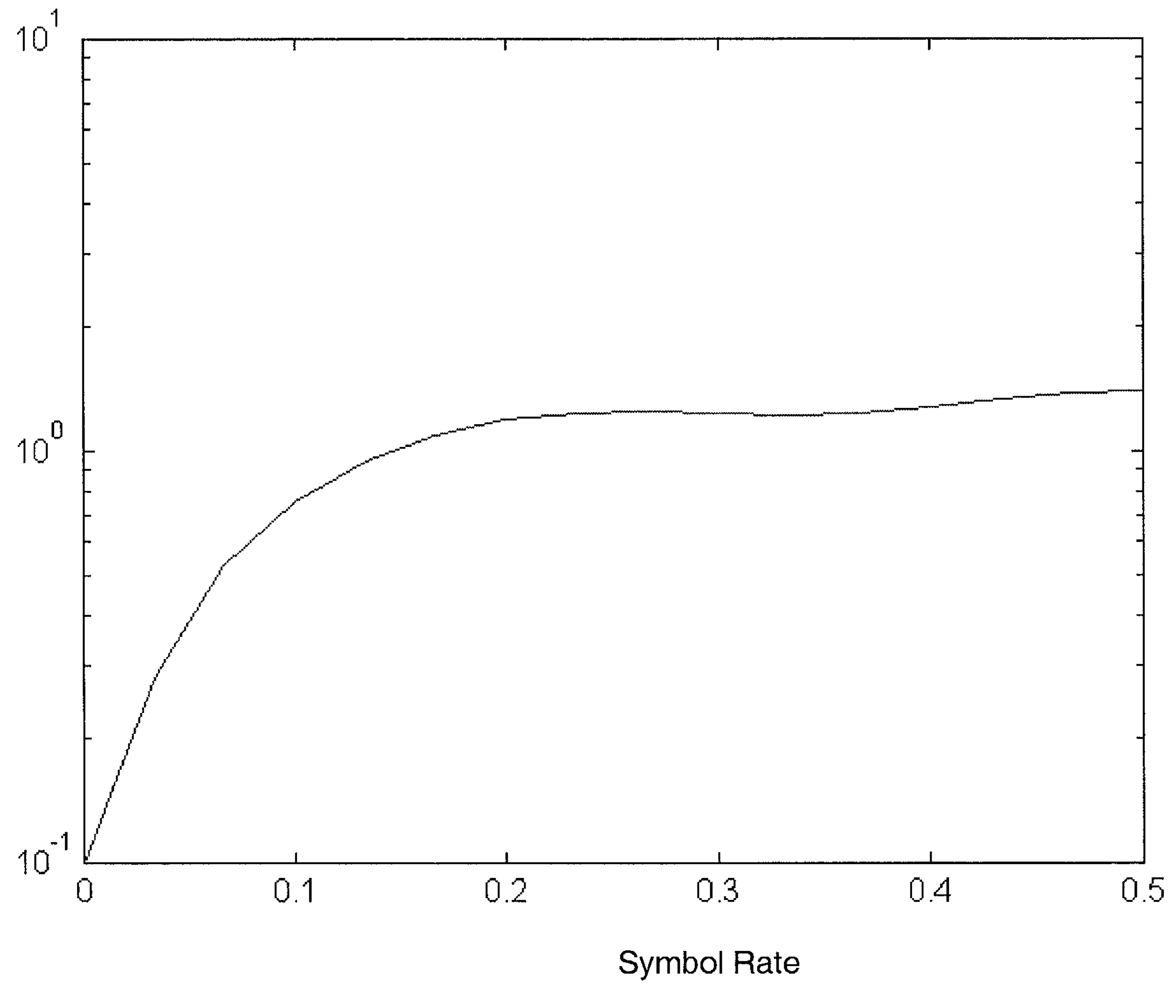

Fig. 5

600

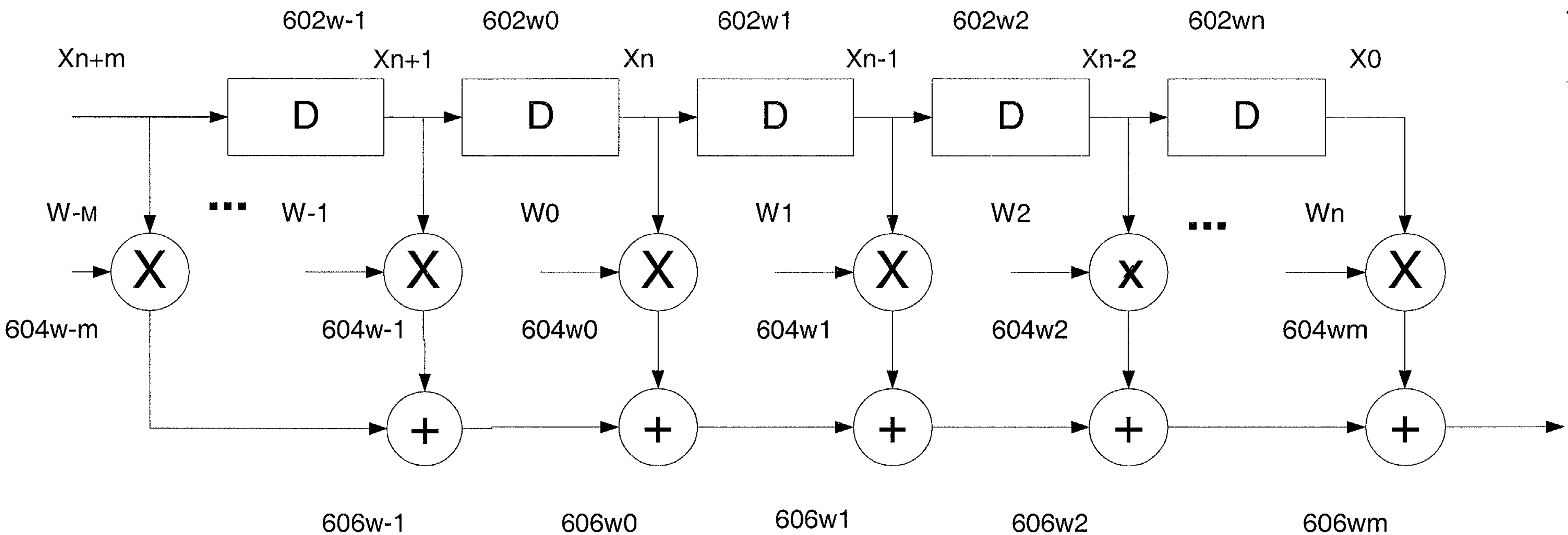
602w-1
602w0
602w1
602w2
602wn
Xn+m
Xn+1
Xn
Xn-1
Xn-2
X0
D
D
D
D
D
W-M
W-1
W0
W1
W2
Wn
X
X
X
X
x
X
604w-m
604w-1
604w0
604w1
604w2
604wm
+
+
+
+
+
606w-1
606w0
606w1
606w2
606wm

Fig. 6

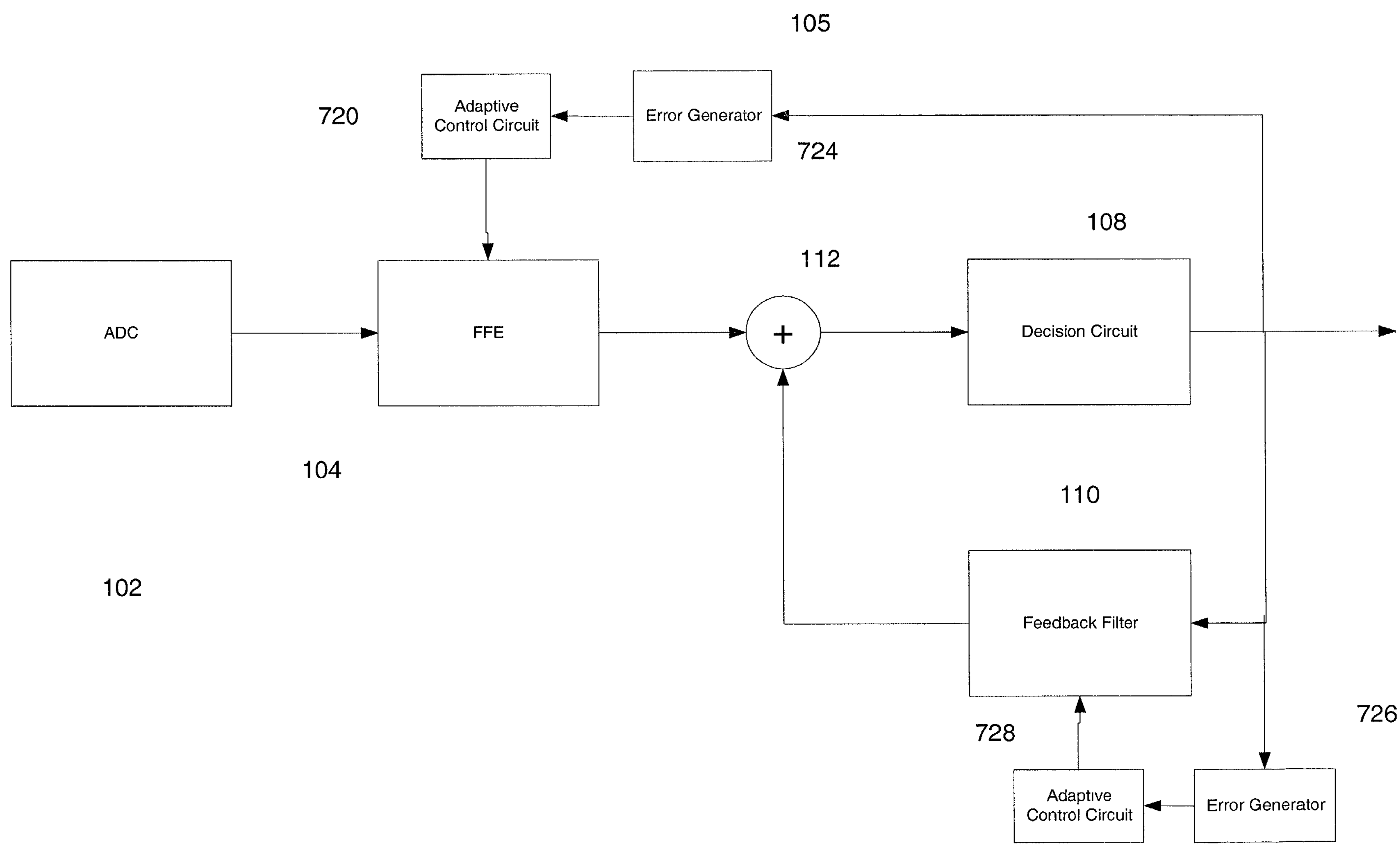
105
720
Adaptive Control Circuit
Error Generator
724
108
112
ADC
FFE
Decision Circuit
+
104
110
102
Feedback Filter
726
728
Adaptive Control Circuit
Error Generator

Fig. 7

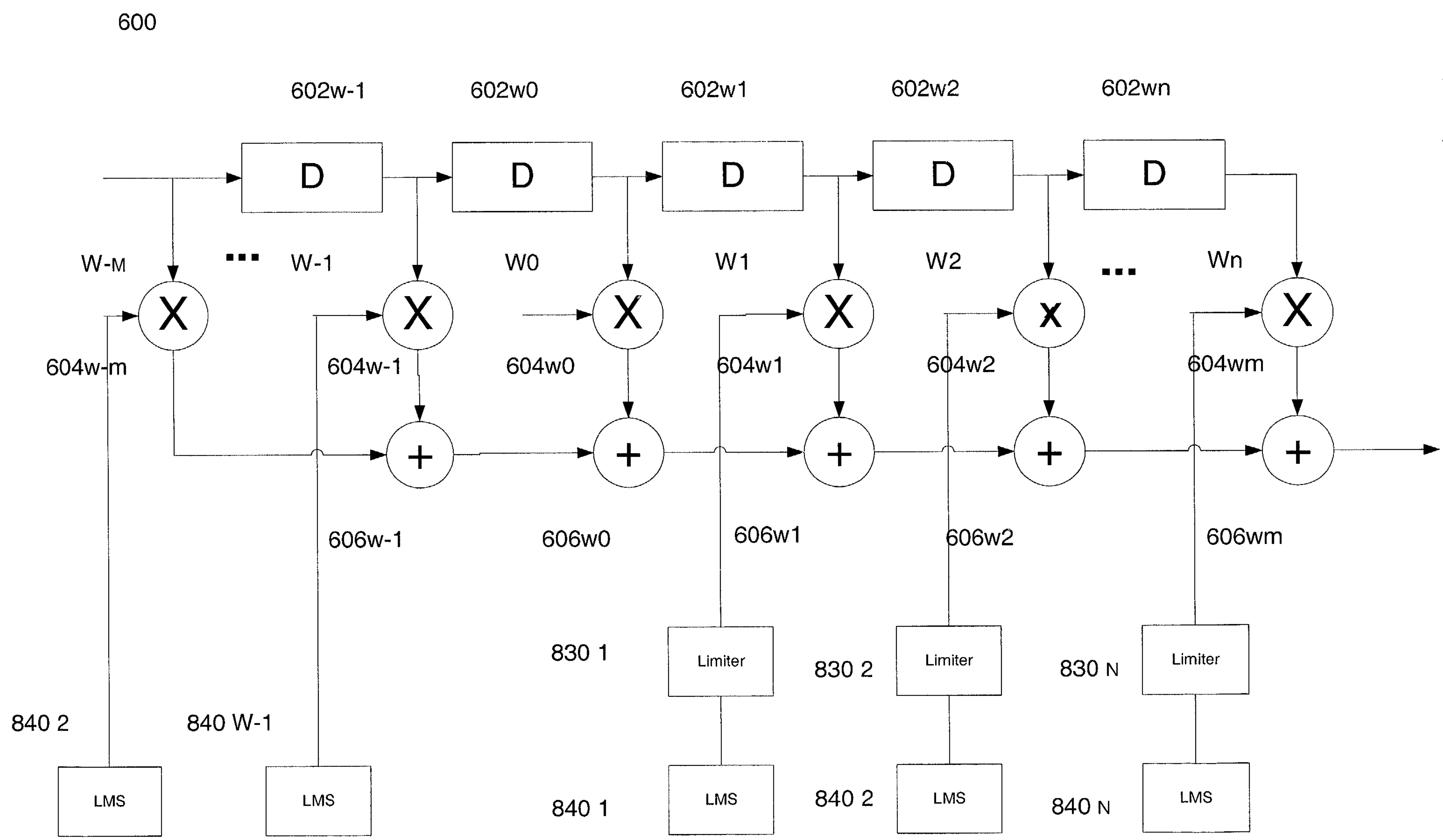
600
602w-1
602w0
602w1
602w2
602wn
D
D
D
D
D
W-M
W-1
W0
W1
W2
Wn
X
X
X
X
x
X
604w-m
604w-1
604w0
604w1
604w2
604wm
+
+
+
+
+
606w-1
606w0
606w1
606w2
606wm
830 1
830 2
830 N
Limiter
Limiter
Limiter
840 2
840 W-1
840 1
840 2
840 N
LMS
LMS
LMS
LMS
LMS

Fig. 8

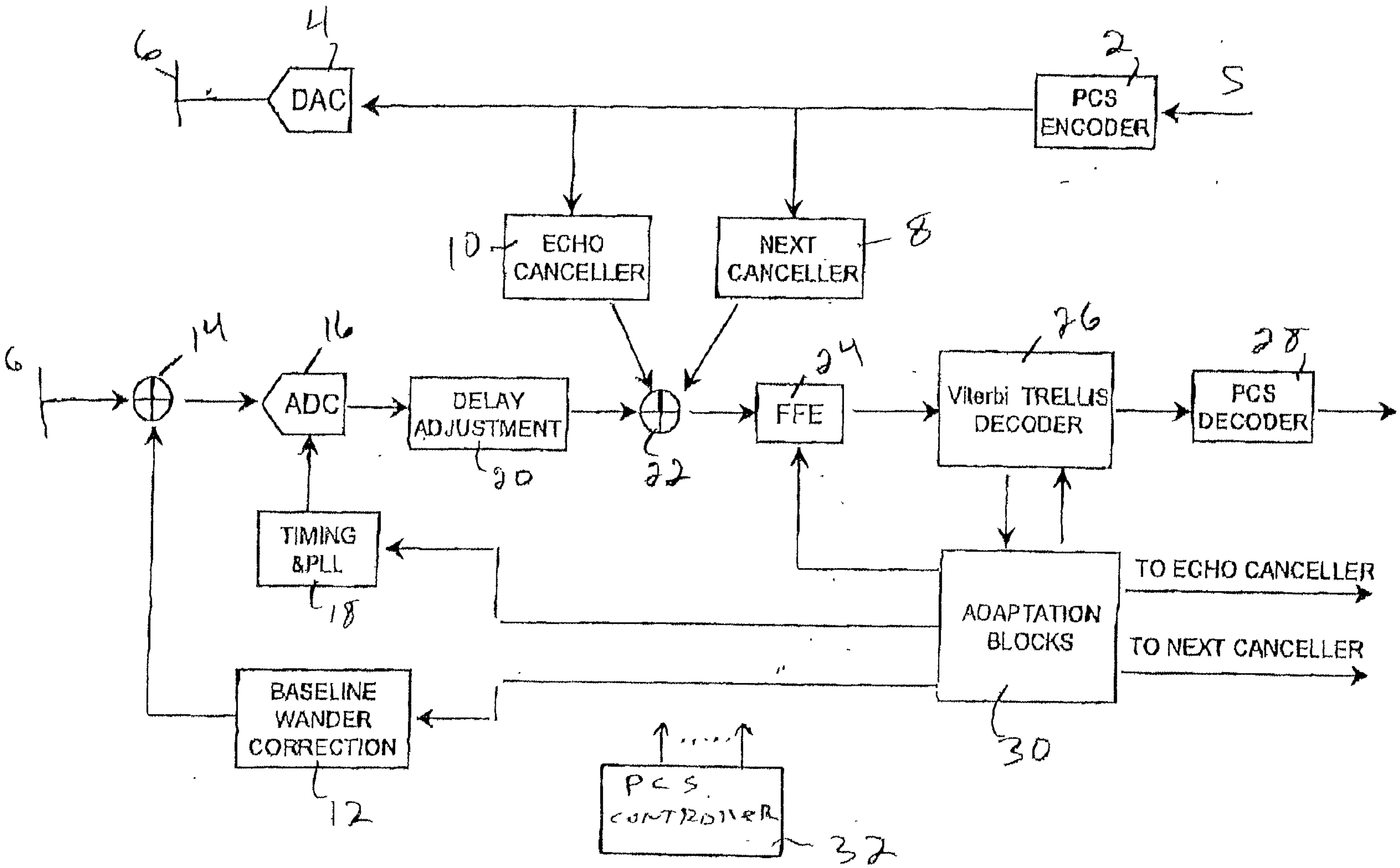
DAC
4
6
PCS ENCODER
2
5
ECHO CANCELLER
10
NEXT CANCELLER
8
6
14
ADC
16
DELAY ADJUSTMENT
20
22
FFE
24
Viterbi TRELLIS DECODER
26
PCS DECODER
28
TIMING &PLL
18
ADAPTATION BLOCKS
30
TO ECHO CANCELLER
TO NEXT CANCELLER
BASELINE WANDER CORRECTION
12
PCS CONTROLLER
32

FIG 9

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(Page 1)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Feedforward Equalizer for DFE Based Detector

☐ the specification of which is attached hereto _X_ was filed on_ as United States Application No. or PCT International Application No._
and was amended on________________________________ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR ' 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. ' 119(a)-(d) or ' 365(b), of any foreign application(s) for patent or inventor's certificate, or ' 365(a) of any PCT international application which designates at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed:

Country	Application No.	Filed (Day/Mo./Yr.)	(Yes/No) Priority Claimed

I hereby claim the benefit under 35 U.S.C. ' 119(e) of any United States provisional application(s) listed below:

Application No.	Filed (Day/Mo./Yr.)

I hereby claim the benefit under 35 U.S.C. ' 120 of any United States application(s), or ' 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. ' 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. ' 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Application No.	Filed (Day/Mo./Yr.)	Status (Patented, Pending, Abandoned)

I hereby appoint the practitioners associated with the firm and Customer Number provided below and Eric B. Janofsky, Reg. No. 30,759 to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to the address associated with that Customer Number:

FITZPATRICK, CELLA, HARPER & SCINTO
Customer Number: 05514

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole or First Inventor Runsheng He

Inventor's signature

Date 08/23/06 Citizen/Subject of People's Republic ofChina

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Post Office Address same